UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,168	07/11/2003	Alan Kyker	42P7938C	4367

8791 7590 12/02/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
MOAZZAMI, NASSER G	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,168	KYKER ET AL.	
	Examiner	Art Unit	
	Nasser G. Moazzami	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,12-15,18-20,22-28 and 30* is/are rejected.

7)☒ Claim(s) *7-11,16,17,21 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Information Disclosure Statement submitted by applicant on 11/13/2003 has been considered. See attached PTO-1449.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 12-15, 18-20, 22-28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) or Quattromani (US Patent No. 5,835,949) in view of Jensen (US Patent No. 5,133,058).

As per claim 1, 19, 23-24, and 27, AAPA discloses an instruction cache 14 that is physically addressed, wherein a snoop is triggered by storing into memory 104 **[page 7, lines 19-20]**, it performs self modifying by comparing the physical addresses stored within the cache **[page 7, lines 20-24]**. AAPA further discloses that when a mach is indicated, the instruction cache is flushed **[page 7, line 25 through page 8, line 1]**.

AAPA discloses the claimed invention, but fails to specifically teach the comparison is within a TLB having a content addressable memory.

Jensen teaches a TLB having a content addressable memory for performing snoop accesses of physical addresses and comparing the physical addresses in the TLB with the physical addresses snooped; the TLB stores page translation between linear addresses and physical pages **[translation look-aside buffer 32 having a portion 52 that may be constructed as a content addressable memory (column 8, lines 16-34); comparator is used to match the physical addresses sought with the physical addresses stored in the TLB (column 9, line 67 through column 10, line 3)]**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the current invention to modify AAPA such that the comparison of the physical addresses occurs in a TLB having a content addressable memory instead the AAPA's instruction cache as being taught by Jensen in order to have a faster system by obviating the problem of time consuming page walks **[column 2, lines 12-43 and column 7, lines 11-12]**.

As for claim 2, AAPA discloses that if it is determined that the physical address received by the TLB matches a physical page address stored within the TLB, indicating that information was modified within the memory correlating to information potentially located within the cache, information within the cache is invalidated **[page 7, line 25 through page 8, line 1]**.

As for claim 3, AAPA discloses that information within the cache is invalidated by setting a bit in the cache to indicate invalid information in a cache line and disregarding the information within the cache **[it is inherent in the art that when a cache line is flushed, the valid bit associated with that line would be set to invalid]**.

As for claims 4, 20 and 28, AAPA discloses that if it is determined that the physical address received by the TLB matches a physical page address stored within the TLB, indicating that information was modified within the memory correlating to information potentially located within the cache or a pipeline, and the microprocessor provides inclusion for the cache and the pipeline such that information within the cache and the pipeline are invalidated **[when an SMC match, the cache memory and instruction pipeline are flushed (page 7, line 25 through page 8, line 1)]**.

As for claim 5, AAPA discloses that information within the cache and a pipeline are invalidated by setting a bit in the cache to indicate invalid information in a cache line and disregarding the information within the cache and the pipeline **[it is inherent in the art that when a cache line is flushed, the valid bit associated with that line would be set to invalid; disregarding the instructions in the pipeline (page 5, lines 1-3)]**.

As for claim 6, AAPA discloses that the TLB maintains original page translations for all bytes of information within the cache and pipeline to provide inclusion

instructions pipeline are guaranteed to stay in the instruction cache (page 7, lines 11-15)].

As for claims 12, 22, and 30 Jensen teaches that the cache is an instruction cache and the TLB is an instruction TLB **[see Fig. 3]**.

As for claim 13, Quattromani discloses an instruction cache which, stores translation between a linear addresses and physical addresses for the cache entries. Quattromani further discloses comparison between the physical address of a write to the physical address tags in the cache to determine if the data stored in the cache memory **[cache 65 (Fig. 5); column 10, lines 14-23 and 39-41]**.

Jensen teaches a TLB having a content addressable memory for performing snoop accesses of physical addresses and comparing the physical addresses in the TLB with the physical addresses snooped; the TLB stores page translation between linear addresses and physical pages **[translation look-aside buffer 32 having a portion 52 that may be constructed as a content addressable memory (column 8, lines 16-34); comparator is used to match the physical addresses sought with the physical addresses stored in the TLB (column 9, line 67 through column 10, line 3)]**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the current invention to modify Quattromani such that the comparison of the physical addresses occurs in a TLB having a content addressable memory instead the AAPA's instruction cache as being taught by Jensen in order to have a faster system by

obviating the problem of time consuming page walks **[column 2, lines 12-43 and column 7, lines 11-12]**.

As for claim 14, Quattromani discloses that the comparing generates a match between the provided physical memory address and one or more of the physical page memory addresses included in the stored page table translations indicating the potential occurrence of self modifying code and cache incoherency **[column 10, lines 21-26 and 39-41]**.

As for claim 15, Quattromani teaches invalidating the instructions within the cache memory and an instruction pipeline for execution and fetching new instructions from the physically addressable memory to overwrite the invalidated instructions after the comparing generates a match indicating the potential occurrence of self modifying code and cache incoherency **[column 10, lines 21-26]**.

As for claim 18, Quattromani teaches maintaining original stored page table translations for all bytes of information within the cache memory and an instruction pipeline **[column 2, lines 33-41]**.

As for claim 23, Quattromani discloses the limitation as set forth for the rejection of claim 13 and in addition discloses that a hit to the physical address in the cache results in invalidation of that entry.

Jensen teaches a TLB having a content addressable memory for performing snoop accesses of physical addresses and comparing the physical addresses in the TLB with the physical addresses snooped; the TLB stores page translation between linear addresses and physical pages **[translation look-aside buffer 32 having a portion 52 that may be constructed as a content addressable memory (column 8, lines 16-34); comparator is used to match the physical addresses sought with the physical addresses stored in the TLB (column 9, line 67 through column 10, line 3)]**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the current invention to modify Quattromani such that the comparison of the physical addresses occurs in a TLB having a content addressable memory instead the AAPA's instruction cache as being taught by Jensen in order to have a faster system by obviating the problem of time consuming page walks **[column 2, lines 12-43 and column 7, lines 11-12]**.

As for claim 25, Quattromani discloses invalidating the information stored into an instruction pipeline from the cache upon generation of the self-modifying code hit signal **[column 10, lines 21-26]**.

As for claim 26, Quattromani discloses fetching instructions from memory to rewrite the information into the cache to obtain cache coherency **[column 10, lines 35-39]**.

Allowable Subject Matter

4. Claims 7-11, 16-17, 21 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nasser G. Moazzami whose telephone number is (571) 272-4195. The examiner can normally be reached on 7:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NASSER MOAZZAMI
PRIMARY EXAMINER
11/23/2005